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DESIGN AND IMPLEMENTATION OF A 2048 - FFT CAPTURE SPECTRUM ANALYZER

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This paper describes the hardware implementation of a digital spectrum analyzer which, by using a capture process of the signal under processing, performs some non parametric signal processing techniques. All the possibilities to implement a spectrum analyzer will arise to a bank filter analysis approach. When the instrument works as an off-line processor, the bank filter can be a linear transform, which results in a FFT as concerns with the analysis of the power density content of the data sample.
Thus the FFT processor can be viewed as a set of equispaced filters with non-ideal cut-off and secondary lobes but optimum to analyze pure tones in a white noise environment.

1. INTRODUCTION

Given a random process x(t) , a way to characterize it is by means the power spectral density. This is an ideal function which relates how the signal power is distributed in the frecuency domain. All the methods for estimating the power spectrum arise from a bank of band-pass filters (although they mustn't be implemented necessarily so). If these filters are signal dependent, parametric methods arise and the non-parametric at any other case. Among the last ones, the most popular are those which make use of the FFT algorithm.

One of these methods is the W.O.S.A. (weighting overlapped spectrum averaging). Analyzer architecture has been designed to acomplish with this method.

The technique to estimate the spectrum by means the W.O.S.A. is the following:

given a signal sample record x(n), $0 \leq n \leq M-1$, it is divided into L segments (with possible overlapping between them) of N points each one. Where N is the FFT size that processes the analyzer. Each segment is windowed (three possible windows are available: rectangular, Barlett and Hanning) and FFT processed. Finally, the modified periodograms are averaged, by means of an uniform or exponential averager, to achieve the spectral estimate.

2. IMPLEMENTATION

For implementing the W.O.S.A. method, several architecture models are employed, which are complexity-price dependents.

If the FFT processor is high speed enough, it could be thought to disposse two memory buffers; while one of them is adquiring signal, the FFT of the other one is evaluated. This is the way in which work real time spectrum analyzers. To achieve real time analysis upon audio frequencies, it is necessary bit-slice techniques and, in any case, the use of special purpose architectures. This is a tradeoff when one is not interested in an expensive instrument.

The other possibility is that of adquiring the signal under test ("capture"), storing it in a memory buffer and estimating the power spectrum density off-line.

An architecture to achieve this idea is much more simple and allows the use of conventional 16 bit microprocessors.

Although a µP design can't achieve real time processing upon a bandwidth of 20 KHz, however it is possible real time processing until 2 KHz (depending upon the speed processing and the FFT size).

Our design is accordingly with this philosophy. For capturing the signal it is provided 20 K word of static RAM. All the associated functions the analyzer achieves are supported in a 2048 sample FFT. It is well known that spectral resolution is closely related to the inverse of the time domain width of the window. So that spectral resolution in the W.O.S.A. method is dependent upon the time duration of the 2048 points. However, because of the 20 K words of signal stored, it is possible throughout the built in "zoom FFT" to achieve a spectral resolution ten times greater the W.O.S.A. Besides, another 12 K word static RAM are supported in the basic model to allow intermediate results. A further enlargement of 32 KW. is foreseen. So it will be possible to store ideal measurements and compare with actual one's.

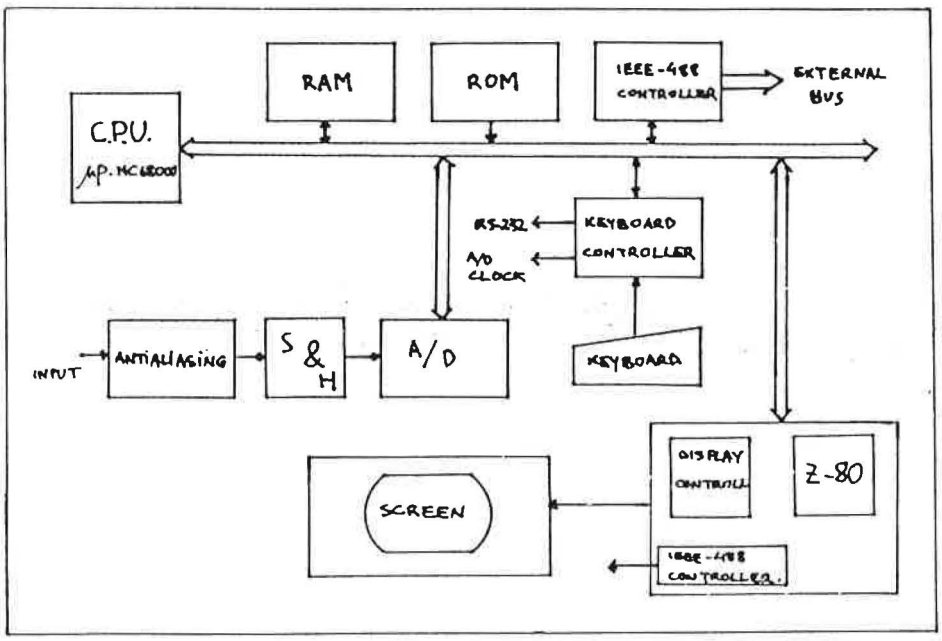

Figure 1. General Block diagram.

The ROM memory unit is also 32 KW size. It isn't too large because datum tables must be stored besides references and program itself.

The adquisition unit consist in an antialiasing analog filter bank (C.C.D); a sample and hold and a 12 bit A/D converter, from which an input dynamic range of about 72 dB is attained.

The analyzer has also been fitted with the IEEE-bus, by means of a bus controller chip. So that, it can work as a peripheric from a host computer

To perform the different processing possibilities, the user manages the analyzer throughout a key board; so that, the hardware design also incorporates a programmable keyboard controller. Among the features of this keyboard controller chip are: to establish serial communications (RS-232) with peripherical devices, as printers or plotters, and also provides a programable tone generator which governs the sample and hold unit.

Graphic results, and different menus are displayed in an intelligent graphic terminal which is μP controlled (by a Z-80 μP). Communications between the CPU and the grafic terminal are also provided throughout the IEEE-bus.

The global architecture of the analyzer can be viewed in figure (1).

In this design, the control unit, so as the computational unit is the μP MC68000. THis CPU disposses of 16 intern registers of 32 bit (8 data registers and 8 address registers).

Interaction between the adquisition unit or the keyboard and the CPU is achieved by interruptions. While the graphic terminal communications and the RS-232 ones (provided by the keyboard controller) are polling performed.

Three internal interrupt levels are allowed. At the higher one, unit adquisition and keyboard are disabled; this corresponds to the CPU processing time. At the next level, unit adquisition is enabled and keyboard disabled and at the third level, keyboard and unit adquisition are enabled, but only keyboard is functionally enabled because the keyboard clock is reset, so the adquisition unit is in idle state.

Communications with a host computer, although, it isn't still software developped, also will

be interrupt performed via the IEEE-bus.

The presentation unit, i.e. the graphic terminal has been designed intelligent (it is supported by a Z-80) to discharge the MC68000 from taskes being not typically computationals. This unit disposses of a graphic screen controller that performs a 512 point resolution in the horizontal axis and 256 point resolution in the vertical one.

It can be seen at figure 1, that no floating-point coprocessor is included. Because of this, all the mathematics operations (either linear or non-linear) must be performed by the 68000 CPU in fixed-point format.

Special routines have been developped to evaluate non-linear mathematics functions: logarithms, exponentials and phases.

Evaluation of that functions is performed with aid fo some significative values which are stored in the ROM memory.

For the logarithm evaluation, it has been implemented the algorithm (1)

$$\log x = \log 2 + \log x/2 \qquad (1)$$

This recursion is followed until x is less or equal than a certain value (1024), in which case, the logarithm value is found at the table.

Exponential recursion is just the inverse than the logarithm one. If x is less than log (1024), then e^x may be obtained directly from the logarithms table; if x is greather than log 1024 it will be $x=n \log 2 + \log u$, where $\log u < \log 1024$, so the problem now is to find $e^{\ln u}$ at the table and finally $e^x=2^n e^{\ln u}$.

For calculating phases, the algorithm followed has been (2)

$$\text{arc tg } x=\pi/2 - \text{arc tg } 1/x; \text{ if } x>1 \qquad (2)$$

If $x<1$ then arc tg x is obtained from tabulated values.

Obviously, since the CPU works over integer numbers, all numbers that are less than one must be left shifted decimal point stored.

Also it is stored in ROM the cosinus and sinus necessary values for computing a 2048 point F.F.T. For computing a 2048 point F.F.T. it is necessary (3).

$$\text{sen } \frac{2\pi i}{2048} \; . \; i = 0,\ldots 1023$$
$$\cos \frac{2\pi i}{2048} \; . \; i = 0,\ldots 1023 \qquad (3)$$

It could be sufficient store (4), i.e. a quadrant

$$\text{sen } \frac{2\pi i}{2048} \quad i = 0,\ldots 511 \qquad (4)$$

But for optimicing execution time it has been tabulated (5)

$$\text{sen } \frac{2\pi i}{2048} \quad i = 0,\ldots 1535 \qquad (5)$$

Indexing from i=0 sinus are obtained and from i=0+512, cosinus do.

Also it has been tabulated the bit-reversed function.

The functions included in software options are: W.O.S.A., signal enhacement, spectrum averaging, zoom-FFT, autocorrelation, Hilbert transform, envelope, instantaneous frequency, minimum phase and complex and real cepstrum. Other graphic features are included which allow on-line signal edition both in time and frequency domain.

It is expected to extend the system for performing two channel signal processing.